الجمـــهورية الجزائريـــة الديمقراطيـــة الشعبيـــة

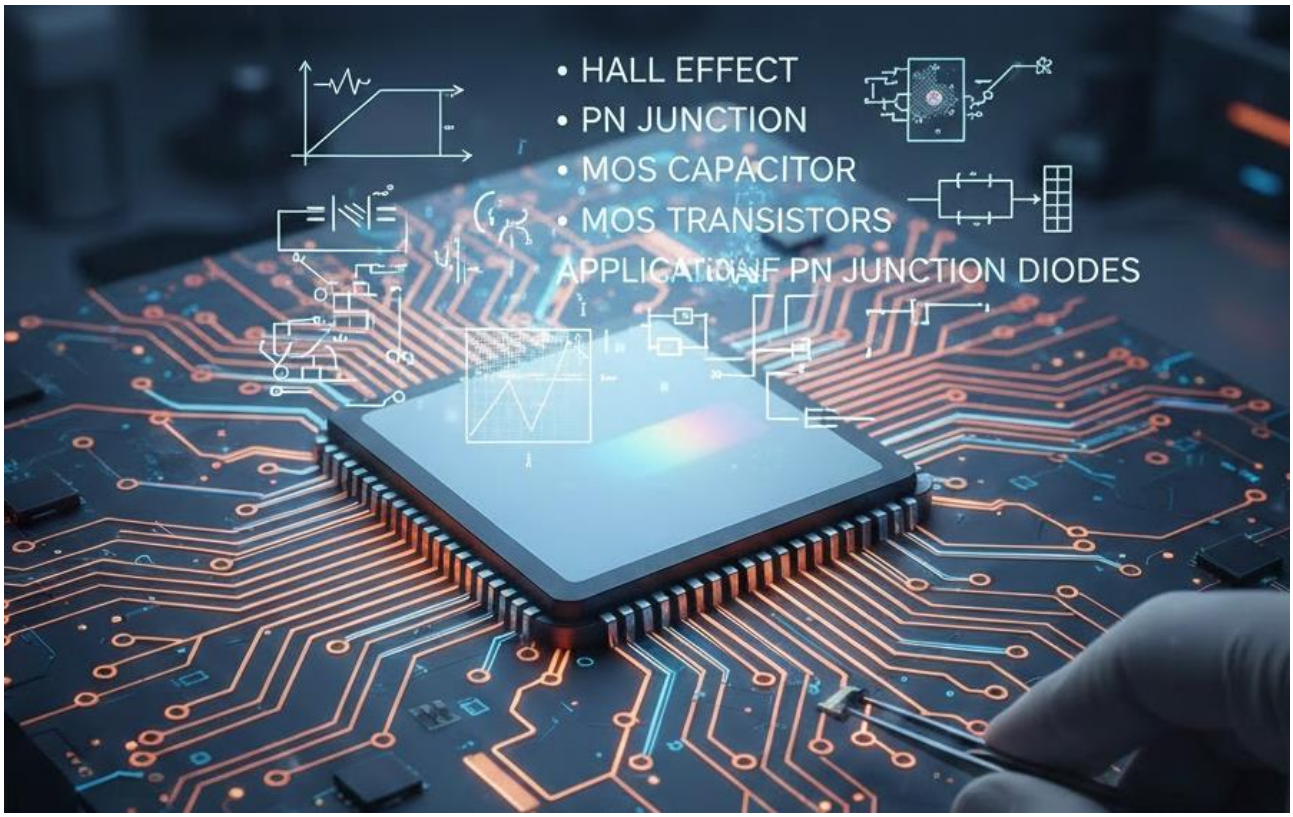
REPUBLIQUE ALGERIENNE DEMOCRATIQUE ET POPULAIRE

Ministère de l'Enseignement Supérieur et de la Recherche Scientifique
Université 8 mai 1945 Guelma
Faculté des Mathématiques et de l'Informatique et des Sciences de la Matière
Département des Sciences de la Matière

وزارة التعليم العالـي و البحث العلمي
جامعة 8 مـاي 1945 قالمـة
كليـة الرياضيات و الإعلام الآلي و علـوم المـادة
قسم علـوم المـادة

POLYCOPY COURSE

Laboratory work in Semiconductor Physics



Designed for students of 3rd year LMD

Materials Physics

Prof. YAHI Hakima

-2026-

Preface

This practical work booklet is intended for third-year LMD undergraduate students in Material Physics, with a focus on Semiconductor Physics. The purpose of the experiments outlined in this booklet is to give students practical experience in understanding the fundamental principles and behavior of semiconductor materials. Through a series of well-structured experiments, students will investigate key concepts such as:

- **Hall Effect:** Generation of a voltage perpendicular to both the current flow and an applied magnetic field in semiconductor, which is used to determine the type and density of charge carriers.
- **PN junction:** The study of PN junction characteristics focuses on the behavior of the junction when a voltage is applied, with the p-side connected to the positive terminal and the n-side to the negative terminal, and vice versa.
- **MOS capacitor:** It refers to the capacitance present in a Metal-Oxide-Semiconductor (MOS) structure, which is crucial to the operation of MOS transistors such as MOSFETs. This capacitance plays a key role in the performance of MOS devices, particularly in high-speed and high-frequency applications.
- **MOS transistors:** Studying MOS transistors (Metal-Oxide-Semiconductor Field-Effect Transistors, or MOSFETs) provides a thorough understanding of their operation, behavior, and practical applications in real-world scenarios.
- **Applications of PN Junction diodes:** The application of PN junction diodes is centered on the experimental analysis of their behavior in various electrical circuits, aiming to understand their functions and practical applications.

As a prerequisite, the knowledge required for the student to easily grasp this unit is closely related to the following subjects: solid-state physics, electronics, optoelectronics, and semiconductor physics.

SYLLABUS

Teaching Unit: UEM
Subject: Semiconductor Physics Practical Work
Field/Discipline/Program: SM/Physics/L3 - Materials Physics
Semester: 6 **Academic year: 2024/2025**
Credits: 2**,** **Coefficient:** 1
Total Weekly Hours: 1h30 min
Course Instructor: YAHI Hakima
Rank: Professor

Objectives:

The semiconductor lab focuses on understanding the electronic properties of semiconductors, including conduction, band structure, and the impact of doping. It also involves experimenting with devices like diodes and transistors and measuring physical phenomena such as the Hall Effect. The goal is to bridge theory with practical applications by observing how semiconductors perform in various circuits and conditions.

Program:

- **Hall Effect**
- **PN junction**
- **MOS capacitor**
- **MOS transistors**
- **Applications of PN Junction diodes**

Assessment: Knowledge check & weightings

Control	Weighting **(%)**
Final Exam	**50**
Report + Laboratory Work	**50**
Total	**100**

Table of Contents

Lab 0
Least Squares Method for Error Calculation

Lab 0: Least Squares Method for Error Calculation

I. Introduction

In experimental sciences, we typically work with two sets of data, denoted {y1, y2, …, yn} and {x1, x2, …, xn}, obtained from measurements. The regression problem consists of determining a potential relationship between the x's and y's, often expressed as y = f(x).

When this relationship is linear, that is, of the form y = ax + b, it is referred to as linear regression. However, even if such a relationship exists, experimental data usually do not perfectly conform to this equation. This is due to the measurement errors inherent in the data.

To account for these uncertainties in the mathematical model, the measured values {y1, y2, …, yn} are often considered as realizations of a random variable Y, and sometimes {x1, x2, …, xn} are also considered as realizations of a random variable X. In this context, Y is called the dependent variable or explained variable, while X is referred to as the independent variable or explanatory variable.

II. Least Squares Line

The data points (xi, yi), where i = 1, 2, …, n, can be represented as a cloud of n points, called a scatter plot, in the (x, y) plane. The centroid of this cloud can be easily calculated; it is the point with the following coordinates:

$$(\bar{x}, \bar{y}) = \left(\frac{\sum_{i=1}^{n} x_i}{n}, \frac{\sum_{i=1}^{n} y_i}{n} \right) \quad (1)$$

$\bar{x}\ and\ \bar{y}$ represent the mean values of x and y, respectively.

Seeking an affine relationship between the variables X and Y involves finding a line that best fits the cloud of points. Among all possible lines, we choose the one with a remarkable property: it minimizes the sum of the squared differences between the observed values yi and the values predicted by the line $\hat{y}_i = ax_i + b$. If ε_i represents this difference, also called the residual, the principle of ordinary least squares (OLS) consists of choosing the values of a and b that minimize the following relation:

$$E = \sum_{i=0}^{n} \varepsilon_i^2 = \sum_{i=0}^{n} \left(y_i - (ax_i - b)\right)^2 \quad (2)$$

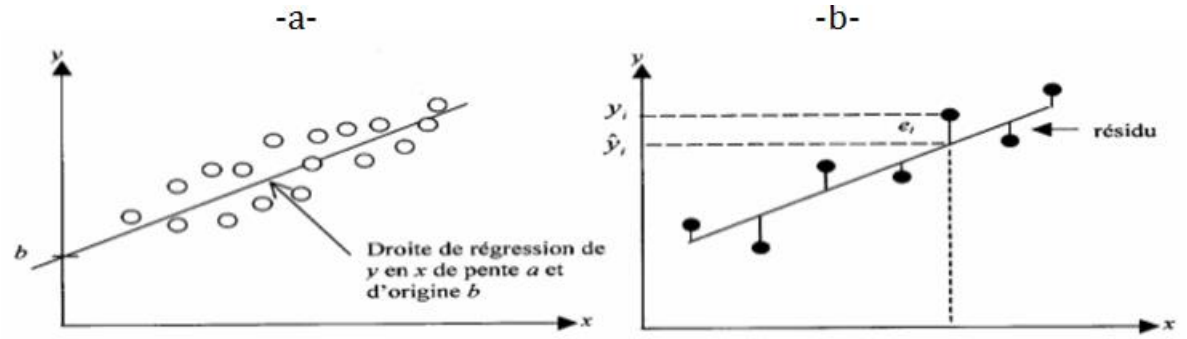


Figure 1: Linear Regression and Residuals, a) Cloud of data points and the regression line, b) Illustration of a residual.

The intercept b is obtained using the following expression:

$$b = \bar{y} - a\bar{x} \quad (3)$$

III. Variance and Covariance

Variance and covariance are two essential statistical measures. The variance describes how much the data are spread around their mean, while the covariance indicates the degree to which two random variables vary together. Although variance is generally intuitive, covariance is defined mathematically in a way that may appear less straightforward at first. In practice, the variance of X, denoted s_x^2, and the covariance between the random variables X and Y, denoted cov_{xy}, are often used to express the coefficient a:

$$a = \frac{cov_{xy}}{s_x^2} \quad (4)$$

with:

$$s_x^2 = \frac{\sum_{i=1}^{n}(x_i - \bar{x})^2}{n} \quad (5)$$

and:

$$cov_{xy} = \frac{\sum_{i=1}^{n}(x_i - \bar{x})(y_i - \bar{y})}{n} \quad (6)$$

IV. Standard Deviation

In mathematics, the standard deviation is a positive real quantity, possibly infinite, used in probability theory to characterize the distribution of a random variable around its mean. The formula for the standard deviation is:

$$\sigma = \sqrt{\frac{\sum_{i=1}^{n} |x_i - \bar{x}|^2}{n}} \tag{7}$$

Therefore, each measured quantity can be presented as:

$$x = \bar{x} \pm \sigma \tag{8}$$

This notation indicates the typical fluctuation of the measurements around the mean value.

Lab 1
Hall Effect

Lab 1: Hall Effect

I. Principle

The Hall Effect occurs when current flows through a conductor or semiconductor placed in a magnetic field perpendicular to the current. The magnetic field causes the charge carriers (electrons or holes) to accumulate on one side of the material, creating a transverse voltage known as the Hall voltage**.**

II. Objectives

- Study of the Hall voltage as a function of the control current, at room temperature and under a uniform and constant magnetic field.
- Study of the voltage across the semiconductor as a function of the magnetic induction, at room temperature and with a constant control current.
- Study of the voltage across the semiconductor as a function of temperature, with a constant control current and in the absence of a magnetic field. The bandgap width is calculated from the measurements.
- Study of the Hall voltage as a function of magnetic induction, at room temperature and with a constant control current. The sign and concentration of charge carriers, the Hall coefficient, and Hall mobility will be determined from the measurements.
- Study of the Hall voltage as a function of temperature, with constant magnetic induction and control current.

III. Theoretical Reminder

If an electric current flows through a semiconductor plate with a rectangular cross-section and thickness d, and if the plate is placed in a magnetic field $\vec{B}$, the field exerts a transverse force on the moving charge carriers, pushing them toward one side of the plate. The resulting magnetic force is called the Lorentz force, given by the equation:

$$\overrightarrow{F_L} = q\left(\vec{v} \times \vec{B}\right) \quad (1)$$

$\vec{v}$ is the drift velocity of the charge carriers, q is their electric charge, and $\vec{B}$ is the magnetic field applied to the semiconductor.

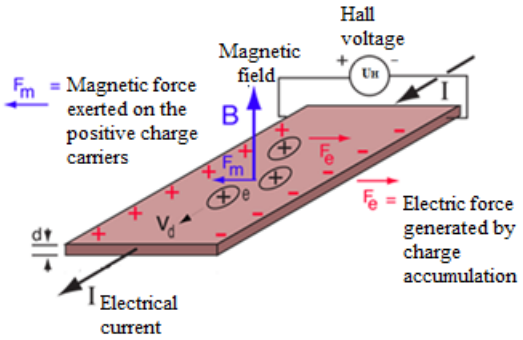


Figure 1: Hall Effect in a rectangular cross-section conductor. The indicated polarity of U_H is for positive charge carriers.

An accumulation of positive or negative charges on the sides of the semiconductor will counterbalance this magnetic influence by generating a measurable voltage across the two sides of the conductor. The presence of this measurable transverse voltage is called the Hall voltage, named after E.H. Hall who discovered it in 1879. The Hall voltage is given by the relation:

$$U_H = \frac{R_H . B . I_p}{d} \tag{2}$$

$$R_H = \frac{1}{n . q} \tag{3}$$

R_H is the Hall constant. The measurement of U_H allows for the determination of the charge carrier concentration n and their sign. It should be noted that the higher the carrier concentration, the smaller the Hall effect. The Hall effect also exists in metals, but it is difficult to measure there because n is too high. In contrast, in semiconductors, where n is lower, U_H is easily measurable. The Hall effect is the method used by manufacturers to measure the carrier concentration in an extrinsic semiconductor.

At high temperatures, the semiconductor enters the intrinsic regime, where the intrinsic conductivity dominates. In this regime, the conductivity is given by:

$$\sigma(T) = \sigma_i \exp\left(-\frac{E_g}{2k_B T}\right) \tag{4}$$

Where k_B = 1.38×10^{-23} J·K^{-1} is the Boltzmann constant, σ_i is the intrinsic conductivity, and E_g is the energy gap of the semiconductor.

Experimentally, the conductivity is obtained from:

$$\sigma = \frac{1}{\rho} = \frac{L}{R.S} = \frac{L.I_p}{U_p.S} \tag{5}$$

which gives:

$$\frac{1}{U_p} = \frac{S}{L.I_p}\sigma \tag{6}$$

where L is the length of the semiconductor, S is its cross-sectional area, I_p is the current, and U_p is the voltage across the sample. The dimensions of the germanium sample are: L×l×d=20×10×1 (mm^3).

The measured voltage U_p at high temperature can therefore be related to the intrinsic law:

$$\frac{1}{U_p} = \frac{S}{L.I_p}\sigma_i \exp\left(-\frac{E_g}{2k_BT}\right) \tag{7}$$

Taking the logarithm gives:

$$ln\frac{1}{U_p} = ln\frac{S.\sigma_i}{L.I_p} - \frac{E_g}{2k_BT} \tag{8}$$

At room temperature, the semiconductor is in the extrinsic regime, and the conductivity measured is therefore:

$$\sigma_0 = \frac{L}{R_0.S} \tag{9}$$

where R_0 is the sample resistance at room temperature and B=0 mT.

Knowing the room-temperature conductivity σ_0, the Hall mobility μ_H of the charge carriers is obtained from:

$$\mu_H = R_H.\sigma_0 \tag{10}$$

IV. Materials and Equipment

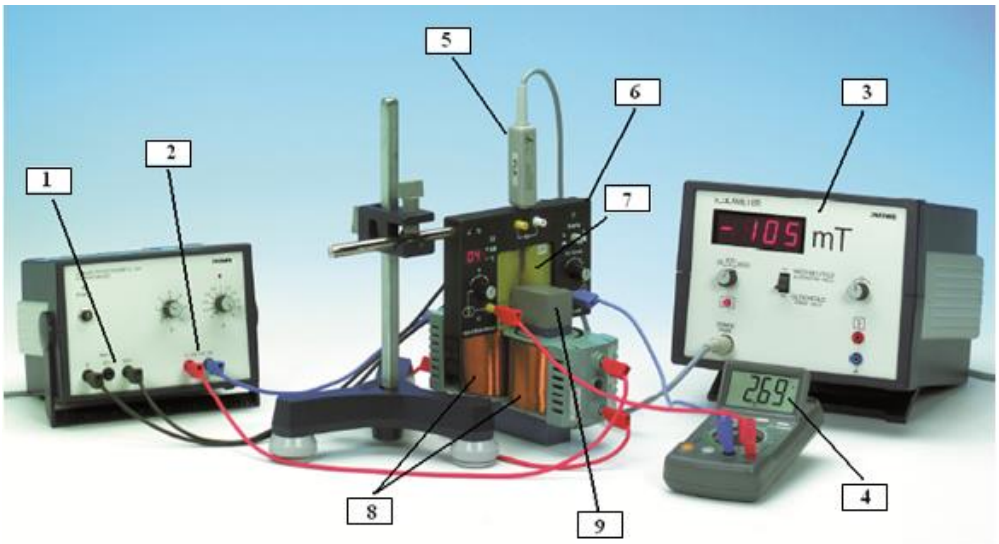


Figure 2: Experimental setup of the Hall effect in semiconductors.

1 - AC power supply for the module,

2 - DC power supply for the electromagnet,

3 - Digital teslameter,

4 - Digital multimeter,

5 - Hall effect probe,

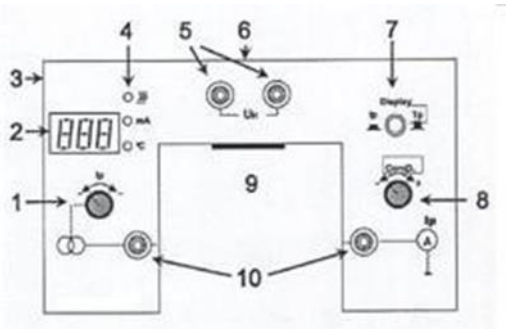
6 - Hall effect module,

7 - Platinum support, Ge-P

8 - 600-turn coils

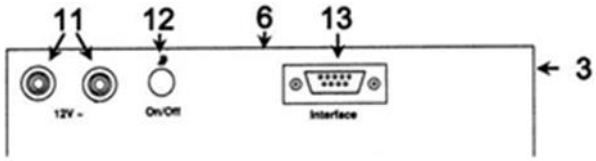
9 - Pole pieces.

Front panel of the Hall Effect module:



1 - Potentiometer for adjusting the current I_p
2 - Display: Current I_p/Temperature
3 - Threaded hole for the support
4 - LED indicator for operating mode
5 - Output sockets for U_H
6 - Slot for the Hall probe
7 - Display selector for I_p/Temperature
8 - Potentiometer for compensating U_H
9 - Socket for removable plates with Ge
10 - Output sockets for U_p across the sample terminals

Rear panel of the Hall Effect module:



11 - 12V AC power input sockets

12 - Heating switch

13 - RS 232 interfaces

V. Procedure

a) Experiment 1

- Assemble the circuit as depicted in Figure 2.
- Adjust the magnetic induction to B=250 mT.
- Connect the multimeter to the Hall voltage output terminals U_H on the front panel of the Hall module.
- Switch the display to current mode, then vary the current I_p flowing through the sample from −30 mA to 30 mA, and measure the corresponding U_H values. Record the results in the table below.

I_p (mA)	–30	–25	–20	–15	–10	–5	0	5	10	15	20	25	30
U_H (mV)													

- Plot the graph of U_H (in mV) versus I_p (in mA).
- Examine the resulting curve and summarize your observations and conclusions.

b) Experiment 2

- Set the current I_p=30 mA.
- Connect the multimeter to the U_p output terminals across the sample.
- Vary the magnetic induction B from 0 to 300 mT and measure the U_p values.
- Enter the measured values in the table below.

B (mT)	0	30	60	90	120	150	180	210	240	270	300
U_p (mV)											
R_m (Ω)											
R_0 (Ω)											
$\left(\frac{R_m - R_0}{R_0}\right)$											

- Plot the curve $[\left(\frac{R_m - R_0}{R_0}\right) = f(B)]$, where R_m is the resistance measured at B≠0, and R_0 is the resistance of the sample when B=0 mT.
- Interpret the curve's shape and discuss how the sample's resistance changes with the magnetic induction B.
- Provide conclusions based on your interpretations.

c) Experiment 3

- Place the Hall Effect module outside the magnetic field (the teslameter should show 0 mT).
- Set the current I_p=30 mA, then use the display selector on the front panel to switch the display to temperature mode.
- Start heating the sample by pressing the "On/Off" button on the rear panel of the module (ensure the temperature does not exceed 140°C).
- Measure the voltage U_p across the sample as the temperature decreases in 10°C intervals.
- Record the measured values in the table below.

T (°C)	140	130	120	110	100	90	80	70	60	50	40	30	20
T^{-1} ($10^{-3}K^{-1}$)													
U_p (V)													
U_p^{-1} (V^{-1})													
$Ln\ (1/U_p)$													

- Plot the curve $[\frac{1}{U_p} = f\left(\frac{1}{T}\right)]$.
- What can be concluded from this curve?
- Plot the curve $[ln\frac{1}{U_p} = f\left(\frac{1}{T}\right)]$.
- What can be concluded from this curve?
- Deduce the values of Eg and σ_0.
- Calculate ΔEg using the least squares method.
- Compare the experimental and theoretical values of σ_0 (given R_0=37.3 Ω).
- Calculate the standard deviation using the least squares method.
- Analyze the results and state your conclusions.

d) Experiment 4

- Set the current I_p=30 mA, and connect the multimeter to the Hall voltage output terminals on the front panel of the module.
- Vary the magnetic induction B from −300 mT to 300mT and measure U_H. Record the measured values in the table below.

Note:

- To obtain negative values of magnetic induction, reverse the polarity on the electromagnet power supply.
- To achieve zero magnetic induction, place the module outside the electromagnet.

B (mT)	–300	–260	–220	–180	–140	–100	–60	–20	0	20	60	100	140	180	220	260	300
U_H (mV)																	

- Plot the graph [$U_H = f(B)$], with U_H in mV and B in mT.
- Analyze the shape of the curve and determine its slope.
- Calculate the standard deviation of the slope.
- Determine the Hall coefficient R_H, and calculate its standard deviation.
- Evaluate the Hall mobility μ_H along with its absolute uncertainty $\Delta\mu_H$.
- Determine the electron concentration n.
- Analyze the results and state your conclusions.

e) Experiment 5

- Set the current I_p to 30 mA and the magnetic induction B to 300 mT.
- Switch the display to temperature mode and start heating the sample by pressing the "On/Off" button on the rear panel of the module (ensure the temperature does not exceed 140°C).
- Measure the Hall voltage U_H as a function of temperature T during the sample's cooling process and record the values in the table below.

T (°C)	140	130	120	110	100	90	80	70	60	50	40	30	20
U_H (mV)													

- Plot the graph U_H as a function of T, with U_H in mV and T in °C.
- Interpret the trend of the curve.
- Analyze the results and state your conclusions.

Lab 2
PN junction

Lab 2: PN junction

I. Principle

The current-voltage characteristics of several PN junctions are measured.

II. Objectives

- Investigation of the variations in the current I_d through Si, Ge, and Zener junctions as a function of the voltage U_d applied across their terminals.
- Plotting the $I_d=f(U_d)$ curves, known as the diode's characteristic, for both forward and reverse bias conditions.
- Determining the load line and identifying the diode's operating point.

III. Theoretical Reminder

A PN junction is created by joining two regions of the same semiconductor material: a P-type region (rich in holes, the majority carriers) and an N-type region (rich in electrons, the majority carriers), as illustrated in Figure 1. This junction forms a boundary called the transition region or depletion region, which separates the P-doped area from the N-doped area. The term "PN junction" specifically refers to this transition zone.

Figure 1 : Schematic representation of a PN junction, showing a P-type semiconductor on the left and an N-type semiconductor on the right. The red lines indicate the depletion region (transition region) between the two doped areas.

The diode is a passive, nonlinear, and polarized component. Its orientation in the circuit is crucial for the correct operation of the electronic system. The diode consists of an anode (A) and a cathode (K), as depicted in the diagram in Figure 2. It is formed by the junction of two semiconductors, one doped with P-type material and the other with N-type material. Current can only flow through the junction from the P region to the N region.

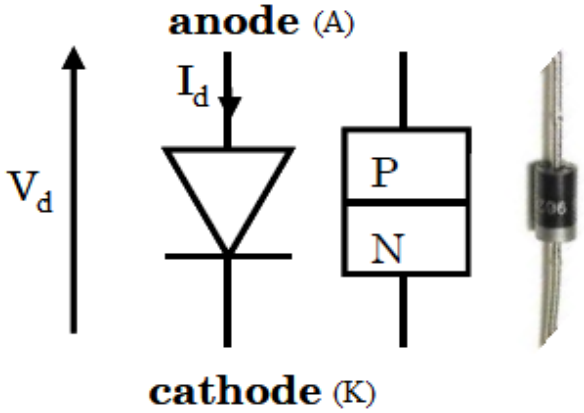


Figure 2: PN junction diode symbol.

The current-voltage characteristic curve of a diode, biased in the forward direction, is given by the relation:

$$I_d = I_s\left(exp\left(\frac{U_d}{n.U_T}\right) - 1\right) \quad (1)$$

Where I_s is the saturation current (the current that flows through the diode when it is reverse biased), typically in the range of nA at room temperature, and U_T is the thermal voltage, given by the relation:

$$U_T = \frac{k_B T}{n.e} \quad (2)$$

Where k_B is the Boltzmann constant, e is the elementary charge, T is the absolute temperature, and n is the diode's constant, which depends on temperature and current intensity. For an ideal junction at room temperature, U_T=26 mV.

The diode is considered forward-biased when the voltage U_d is positive. The threshold voltage U_{th} for a silicon diode typically ranges between 0.6 V and 0.7 V. When U_d is negative, the diode is reverse-biased, and the current flowing through it is very small. However, if the reverse voltage increases enough, to reach a specific value known as the breakdown voltage, the current increases rapidly and damages the diode.

The load line defines the operating point of a component within a given circuit. To determine the load line (Figure 3) of the electrical circuit shown in the diagram of Figure 4, the following steps are performed:

1. Write the Kirchhoff's voltage law for the circuit used.
2. Consider the limiting cases where the diode creates a short circuit (I_d=0), and the case where the diode creates an open circuit (U_d=0).
3. The operating point of the diode corresponds to the point of intersection between the characteristic curve $I_d = f(U_d)$ and the load line of the circuit (see Figure 3).

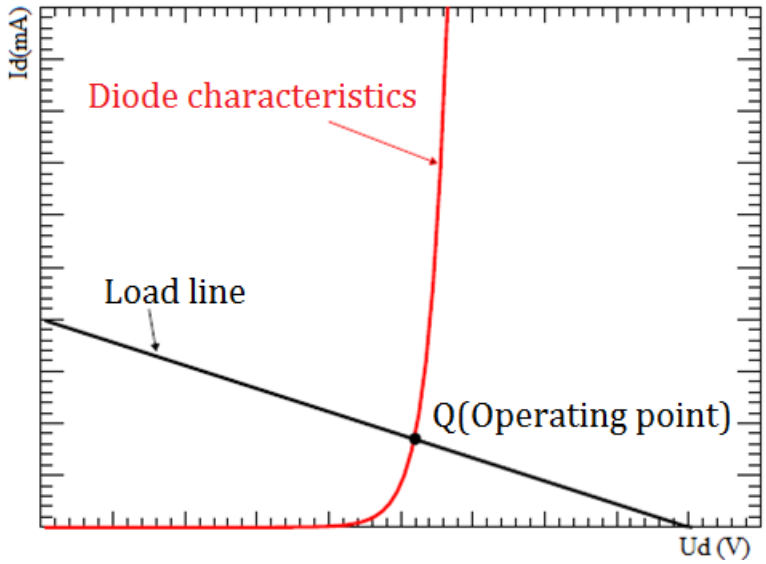


Figure 3: Representation of the load line and the operating point of a forward-biased diode.

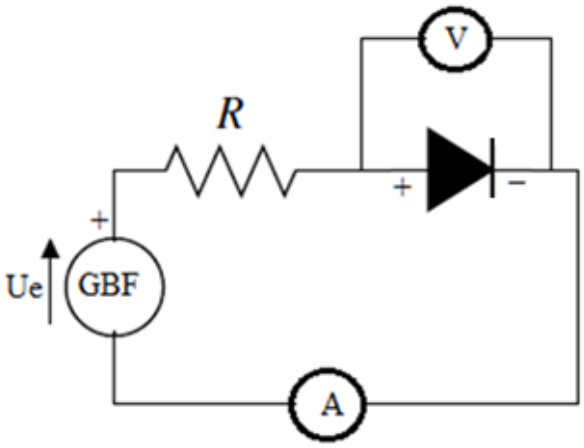


Figure 4: Electrical circuit of a forward-biased diode.

The dynamic resistance of a diode (Figure 5) is the inverse of the slope and is defined by the formula:

$$R_d = \frac{\Delta U_d}{\Delta I_d} \qquad (3)$$

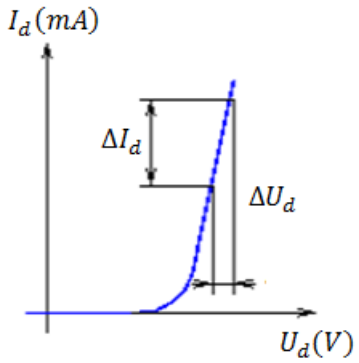


Figure 5: Determination of the dynamic resistance from the (I_d, U_d) characteristic of a forward-biased diode.

A Zener diode consists of a junction between N-type and P-type semiconductors. When the P-N junction is thin and the doping level is high, the diode exhibits a strong reverse current once the reverse voltage exceeds a specific value U_Z, known as the Zener voltage.

Unlike conventional diodes, which only conduct in the forward direction, Zener diodes are designed to also allow current flow in the reverse direction, but only when the voltage across them surpasses the avalanche breakdown threshold.

As the reverse voltage increases, the internal electric field, at the P-N junction, strengthens, giving minority charge carriers enough energy to generate additional carriers through impact ionization. This results in a rapid increase in reverse current due to the avalanche effect, which can damage the diode if not controlled by a series resistor. Consequently, the Zener diode is capable of sustaining a significant reverse current.

Figure 6: Zener diode symbol.

IV. Materials and Equipment

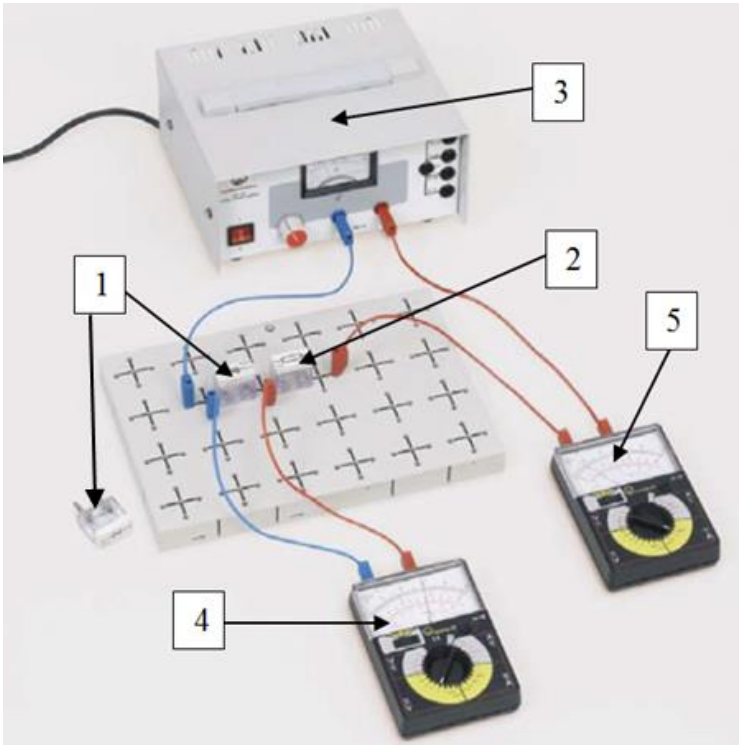


Figure 7: Experimental setup.

1. Si-1N4007, Ge-AA118, ZPD 6.2, and ZPD 9.1 diodes.
2. 100 Ω resistor.
3. 0-12V AC/DC power supply.
4. Voltmeter.
5. Ammeter.

V. Procedure

a. Experiment 1

- Assemble the electrical circuit as shown in Figure 4, first placing the Si-1N4007 diode and then the Ge-AA118 diode, both in forward bias.
- What is the purpose of the resistor R in the circuit?
- Adjust the input voltage Ue of the function generator to fill in the measurement table below. Make sure not to exceed the maximum current of 30 mA that the diode can tolerate.

Si-1N4007	U_d (V)										
	I_d (mA)										
Ge-AA118	U_d (V)										
	I_d (mA)										

- Plot both characteristic curves $I_d=f(U_d)$ on a single graph and analyze the shape of both curves.
- Using the curves, determine the threshold voltage U_{th} for both diodes, where the current starts to flow noticeably.
- Draw the load lines and, by graphical means, determine the operating point of both diodes for two different input voltages: Ue=2V and Ue=4V. What do you observe?
- Calculate the dynamic resistances R_d of both diodes at their operating points for the input voltage Ue=4V. What do you notice?
- Redraw the characteristic $ln(I_d)=f(U_d)$ for both diodes on a separate graph. What is the slope of each curve?
- Calculate the saturation current I_S and the value of the product $n \cdot U_T$, then deduce the factor n (using the least squares method).
- Provide conclusions based on your interpretations.

b) Experiment 2

- Set up the electrical circuit as shown in Figure 8, this time placing the Si-1N4007 diode first, followed by the Ge-AA118 diode, both in reverse bias.
- Why was the resistor R removed from the circuit?

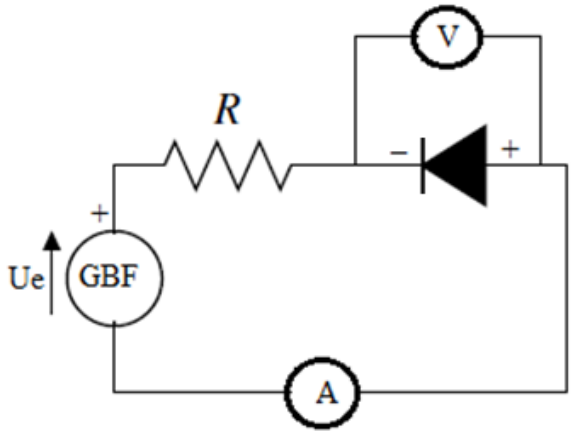


Figure 8: Electrical circuit of a reverse-biased diode.

- Vary the input voltage Ue of the function generator to complete the measurement table below.

Si-1N4007	U_d (V)								
	I_d (mA)								
Ge-AA118	U_d (V)								
	I_d (mA)								

- Plot both characteristic curves $I_d = f(U_d)$ on the first graph.
- Comment on the shape of the two curves.
- Conclude with interpretations.

c) Experiment 3

- Set up the electrical circuit as shown in Figure 9, placing the Zener diode ZPD 6.2 first, followed by the Zener diode ZPD 9.1, both in forward bias.

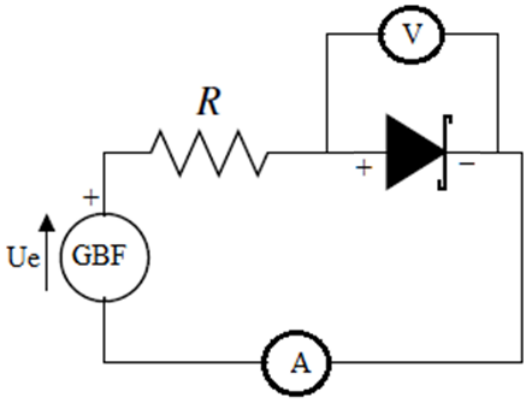


Figure 9: Electrical circuit of a forward-biased Zener diode.

- Why is there a resistor R in the circuit?
- Vary the input voltage Ue of the function generator to complete the measurement table below. Be careful not to exceed the maximum current of 30 mA that the diode can tolerate.

ZPD 6.2	U_d (V)									
	I_d (mA)									
ZPD 9.1	U_d (V)									
	I_d (mA)									

- Plot both characteristic curves $I_d=f(U_d)$ on a single graph.
- Comment on the shape of the two curves.
- From the curves, determine the threshold voltage U_{th} of the two Zener diodes, where the current starts to flow significantly. What do you observe?
- Determine the dynamic resistances R_d of both diodes in forward bias when the curves are linear. What do you observe?
- Conclude with interpretations.

d) Experiment 4

- Set up the electrical circuit as shown in Figure 10, placing the Zener diode ZPD 6.2 first, followed by the Zener diode ZPD 9.1, both in reverse bias.
- Why was the resistor R not removed from the circuit?

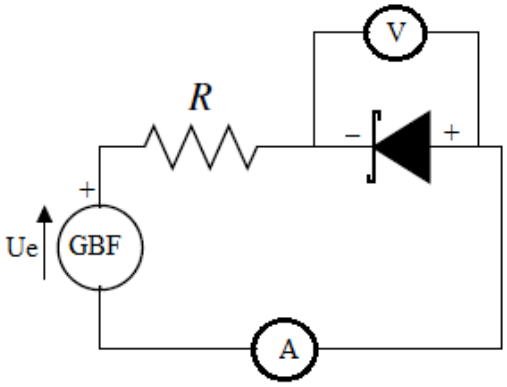


Figure 10: Electrical circuit of a reverse-biased Zener diode.

- Vary the input voltage Ue of the function generator to complete the measurement table below. Be careful not to exceed the maximum current of 30 mA that the diode can tolerate.

ZPD 6.2	U_d (V)									
	I_d (mA)									
ZPD 9.1	U_d (V)									
	I_d (mA)									

- Plot both characteristic curves $I_d=f(U_d)$ on the first graph.
- Comment on the shape of the two curves.
- From the graph, determine for both Zener diodes the voltage $U_Z<0$ at which the diode starts conducting again in the reverse direction. U_Z is the Zener voltage.
- Draw the load lines for an input voltage Ue=4V, ensuring the diodes are reverse biased and a current flows. Deduce the operating point for each Zener diode. What do you observe?
- Determine the dynamic resistances R_{di} of the diodes in reverse bias when the curves are linear. What do you notice?
- Conclude with interpretations.

Lab 3
MOS capacitor

Lab 3: MOS capacitor

I. Principle

The MOS capacitor is composed of a metal gate, an oxide layer, and a semiconductor substrate. Its operation relies on the electrostatic control of charge carriers in the semiconductor by applying an external voltage to the metal gate. This applied voltage affects the charge distribution within the semiconductor, resulting in three distinct operating modes: Accumulation, Depletion, and Inversion.

II. Objectives

- Study the capacitance-voltage (C-V) curve of a MOS capacitor.
- Determine the threshold voltage (V_{th}) of the MOS device.
- Calculate the gate oxide thickness from the capacitance-voltage measurements.
- Analyze the effects of the substrate doping on the electrical characteristics of the MOS.
- Observe the three operating modes (accumulation, depletion, inversion) of the MOS through the variations in capacitance.

III. Theoretical Reminder

An MOS capacitor consists of a semiconductor substrate, an insulating layer such as SiO2, and a metal electrode known as the gate. The oxide layer can be as thin as 1.5 nm.

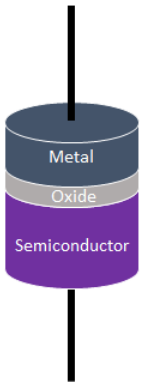


Figure 1: The MOS capacitor.

When a voltage is applied to the metal, it induces either positive (holes) or negative (electrons) charges on the semiconductor surface. Opposite charges accumulate on the metal plate, causing the structure to function as a capacitor.

Figure 2 illustrates the fundamental structure of a Metal-Oxide-Semiconductor (MOS) capacitor, which is built upon a Silicon substrate, the base semiconductor material, typically either p-type or n-type. The structure is composed of three distinct layers:

- Gate Electrode is the top conducting layer. It is usually made from a highly conductive material like aluminum (metal) or heavily doped polysilicon.

- Silicon Dioxide (SiO_2) is the insulating layer (dielectric). It has a specific thickness, labeled as t_{ox}, and its primary role is to electrically separate the gate electrode from the silicon substrate, thus forming the crucial oxide component of the MOS structure.

- Silicon Substrate is the foundational layer of the Metal-Oxide-Semiconductor (MOS) capacitor and serves as the semiconductor body where all charge control ultimately takes place.

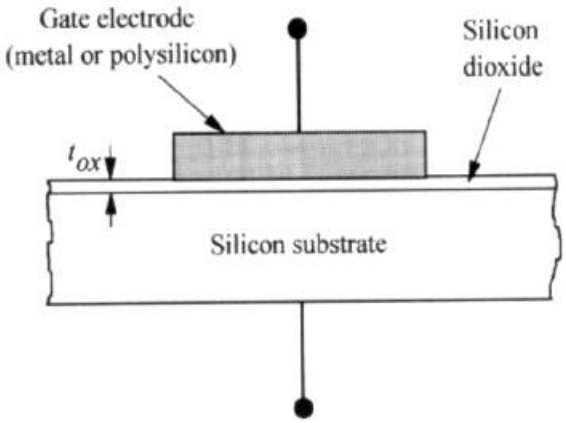


Figure 2: MOS capacitor structure.

Figure 3 represents the energy band structure diagram of the MOS system in equilibrium (zero bias), where a Schottky barrier is formed ($\Phi_M > \Phi_{SC}$).

- Metal and SC(n) are the metal and n-type semiconductor contacts.

- E_F (Red dashed line) is the Fermi energy level, representing the constant electrochemical potential of electrons aligned across the entire junction at equilibrium.

- E_C (Dashed line) is the conduction band minimum, which is the lowest energy level available for electrons in the semiconductor's conduction band.

- E_V (Solid line) is the valence band maximum, the highest energy level available for electrons in the semiconductor's valence band.

- $e\Phi_M$ is the metal work function, defined as the energy difference between the vacuum level and the metal's Fermi level (E_F).

- $e\Phi_{SC}$ is the semiconductor work function , defined as the energy difference between the vacuum level and the bulk Fermi level (E_F) of the semiconductor.

- $e\chi_{SC}$ is the semiconductor electron affinity , representing the energy difference between the vacuum level and the semiconductor's conduction band minimum (E_C).

- eV_d (or eV_{bi}) is the built-in potential energy. This term describes the total potential energy barrier that is created across the depletion region in the semiconductor, causing the characteristic band bending shown in the diagram.

- dx specifies the width of the depletion region, which is the spatial extent of the space-charge region within the semiconductor.

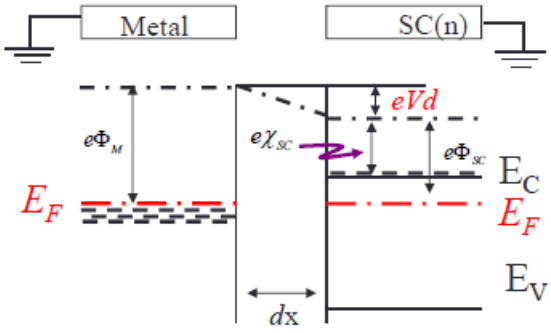


Figure 3: Equilibrium energy band diagram of the MOS system.

The operation of a MOS capacitor depends on the type (doping) of the semiconductor and the voltage applied to the metal gate, resulting in three distinct modes. In one mode, the voltage applied to the metal gate causes the accumulation of majority carriers on the semiconductor surface, known as "Accumulation." In another mode, the applied voltage induces minority carriers on the surface, initially creating a depletion region (the "Depletion" mode). Eventually, this leads to the

inversion of the majority carrier type at the surface, which is referred to as "Inversion." In both accumulation and strong inversion, the MOS capacitor behaves like a typical parallel plate capacitor with constant capacitance. However, in depletion mode, the width of the depletion region influences the capacitance, making it dependent on the applied bias.

The capacitance–voltage (C–V) measurement is an effective and widely used technique for determining parameters such as the gate oxide thickness, substrate doping concentration, threshold voltage, and flat-band voltage.

The C–V curve is typically measured using a C–V meter (Fig. 4), which applies a DC bias voltage, Vg, along with a small sinusoidal signal (ranging frequencies from 1 kHz to 10 MHz) to the MOS capacitor, while measuring the capacitive current with an AC ammeter. The capacitance is then calculated using the formula:

$$\omega . C = \frac{i_{cap}}{v_{ac}} \tag{1}$$

Where ω is the angular frequency ($\omega=2\pi f$), i_{cap} is the magnitude of the measured current through the capacitance, and v_{ac} is the magnitude of the sinusoidal AC voltage signal.

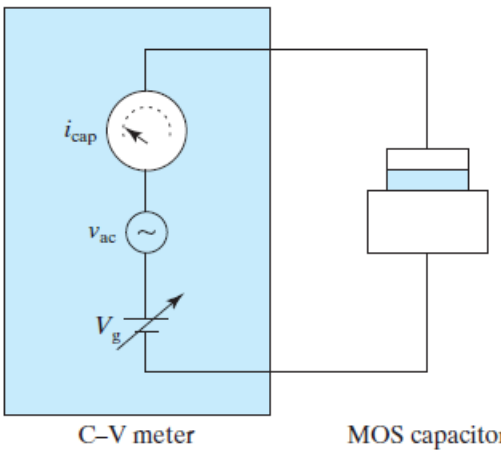


Figure 4: C–V Measurement Setup for a MOS Capacitor.
A C–V meter applies a DC gate voltage V_g combined with a small AC signal v_{ac} to the MOS capacitor. The resulting capacitive current i_{cap} is measured, allowing the capacitance of the MOS structure to be extracted.

In accumulation and strong inversion, the capacitance of the MOS capacitor can be approximated to be:

$$C_{a/i} = C_{ox} = \frac{\varepsilon_{ins} A}{d} \tag{2}$$

$C_{a/i}$ is the capacitance measured in accumulation or inversion (high-frequency), where the MOS capacitor behaves like a simple oxide capacitor, C_{ox} is the capacitance of the insulating layer separating the gate from the semiconductor, ε_{ins} is the dielectric constant of the insulator, A is the surface area, and d is the thikness of the insulating layer.

In depletion, the capacitance C_d of the MOS capacitor depends on the thickness of the depletion region and becomes smallest at the maximum width of the depletion region. The minimum capacitance of the MOS capacitor, just before it switches from depletion to inversion can be approximated by:

$$C_d = \frac{\varepsilon_{ins} A}{W_m} \tag{3}$$

$$W_m = 2\left[\frac{2\varepsilon_{ins}\phi_{s,inv}}{qN_{A/D}}\right]^{1/2} \tag{4}$$

where, W_m is the maximum width of the depletion region, $\phi_{s,inv}$ is the surface potential at the beginning of inversion and $N_{A/D}$ is the doping concentration of the semiconductor.

In the static case and at low operating frequencies, the capacitance values can be expressed using the analytic expressions given in Eq. 2 and Eq. 3. In accumulation and depletion, the charge movement in the semiconductor is carried by majority carriers. Their response is limited by the semiconductor's dielectric relaxation time, which is extremely short, making their motion very fast. The high frequency capacitance of the MOS capacitor in accumulation and depletion region therefore follows their static values. In inversion however, the inversion layer is separated from the bulk semiconductor by the depletion region and the movement of charge at the surface is restricted by the generation rate of the carriers. Thus the inversion capacitance becomes smaller at high frequency and becomes almost equal to the minimum capacitance of the MOS capacitor.

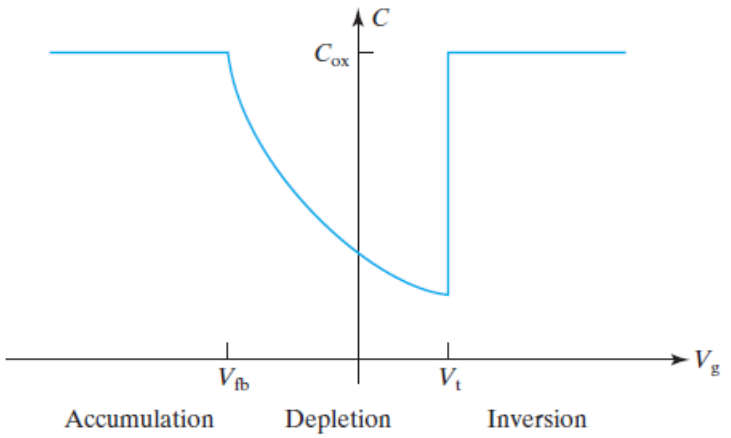


Figure 5: Low-frequency C–V characteristic of a MOS capacitor.
The capacitance remains equal to the oxide capacitance C_{ox} in accumulation, decreases in the depletion region as the depletion width increases, and returns to C_{ox} in strong inversion. The flat-band voltage V_{fb} and threshold voltage V_t mark the transitions between these regimes.

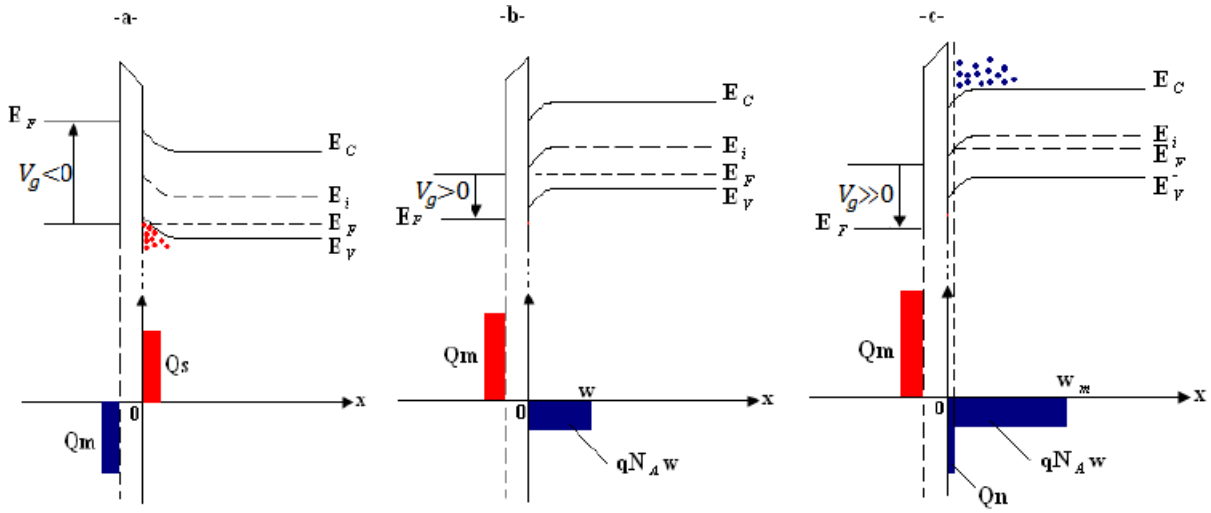


Figure 6: Energy-band diagrams and charge distributions in an ideal MOS structure in the three operating regimes, (a) Accumulation**:** A negative gate voltage bends the energy bands downward, attracting majority carriers (holes, indicated by red dots) at the semiconductor surface and producing a positive surface charge Qs. (b) Depletion: A small positive gate voltage bends the bands upward, creating a depletion region of width w with ionized acceptor charge qN_Aw. (c) Inversion: A larger positive gate voltage further increases band bending, forming an inversion layer of minority carriers (electrons, indicated by blue dots) at the surface in addition to the depletion charge. Qm and Qn are the metal and inversion layer charge, respectively.

IV. Materials and Equipment

1. MOS capacitor.
2. DC voltage source (Vg) to apply bias to the gate.
3. Signal generator.
4. C–V meter or capacitance meter.
5. AC ammeter to measure the capacitive current.
6. DC power supply to apply the bias voltage.

V. Procedure

- Apply a DC voltage (Vg) to the gate using a DC power supply (Start with a negative gate voltage (or positive, depending on the type of semiconductor) and measure the capacitance at different Vg values).
- Superimpose a small sinusoidal AC voltage (typically between 1 kHz and 10 MHz) onto the DC voltage using a signal generator.
- The variation in the applied voltage (Vg) induces a capacitive response, which is measured using a C-V meter or a capacitance meter (Ensure that the C-V meter is properly calibrated and that the amplitude of the AC signal is low enough not to disturb the behavior of the MOS).
- The capacitive current, which depends on the frequency of the AC signal, can be measured with an AC ammeter and used to calculate the capacitance using the formula (1).
- Measure the capacitance as a function of the applied voltage (Vg) to obtain the C-V curve.
- Plot the C-V curve by recording the capacitance for different Vg values. The resulting curve should show three characteristic regions: accumulation, depletion, and inversion.
- By analyzing this curve, you will be able to deduce important parameters such as the threshold voltage (V_{th}), capacitance in accumulation, capacitance in inversion, capacitance in depletion mode, the oxide thickness, and the substrate doping concentration.
- Explain discrepancies due to process variations or measurement errors.
- Evaluate how frequency affects the measured capacitance.

Lab 4
MOS transistors

Lab 4: MOS transistors

I. Principle

The MOS transistor, commonly referred to as a MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), is a type of field-effect transistor that controls the conductivity of a semiconductor channel by applying a voltage to the gate**.** Thanks to its low power consumption, it is extensively used in both digital and analog electronics, serving as both a switch and an amplifier**.**

II. Objectives

- Studying the I-V Characteristics:
- Determining the Threshold Voltage (V_{th}):
- Analyzing the MOSFET in Different Modes:
- Extracting Transistor Parameters:

III. Theoretical Reminder

A MOS transistor (implicitly a MOSFET: Metal-Oxide-Semiconductor Field-Effect Transistor) is a component with four connectors called: Gate (G)**,** Drain (D)**,** Source (S)**,** and Substrate (Sub)**.** In practice, only three terminals are typically used: the gate, drain, and source, with the substrate usually connected to the source.

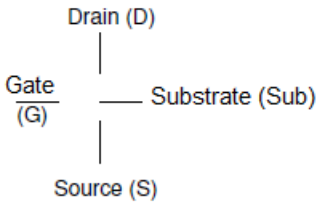


Figure 1: The various terminals of a MOS transistor.

There are four types of MOS transistors, depending on the type of channel and the state of the channel when the transistor is off:

- **N-channel, Normally ON**: The channel is of N-type, and the doping is such that the channel exists without any applied voltage (hence the term "Normally ON"). This type of transistor is also called NMOS depletion-mode **(or** NMOS depletion-type**).**
- **N-channel, Normally OFF**: The channel is of N-type, and the doping is such that the gate-source (GS) junction must be biased to form the channel. This type is also called NMOS enhancement-mode**.**
- **P-channel, Normally ON**: The channel is of P-type, and the doping is such that the channel exists without any applied voltage (hence the term "Normally ON"). This type of transistor is also known as PMOS depletion-mode **(or** PMOS depletion-type**),** though it is rarely used.
- **P-channel, Normally OFF**: The channel is of P-type, and the doping is such that the gate-source (GS) junction must be biased to form the channel. This type is also called PMOS enhancement-mode**.**

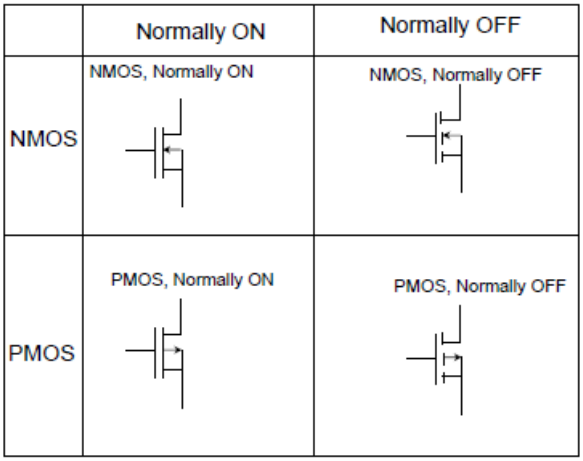


Figure 2: Symbols of the four types of MOS transistors.

At equilibrium, no channel is formed: a long P-type region separates the two N-type regions (Source and Drain). As a result, no current can flow between the source and drain near equilibrium. The structure resembles a vertically oriented MOS capacitor between the source and drain, which enables channel control.

The control voltages are as follows:

- $\mathbf{V_{GS}}$ (corresponding to Vtrans) regulates the channel through the MOS capacitor, determining its existence and cross-section.
- $\mathbf{V_{DS}}$ (corresponding to V_{long}) facilitates electron flow through the channel, as the applied electric field accelerates the electrons.

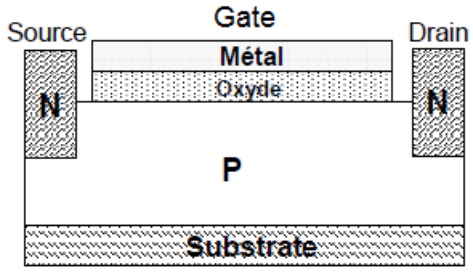


Figure 3: MOS Transistor in equilibrium.

In the linear regime, the source and substrate are connected to ground, and a V_{GS} voltage is applied (with a small positive V_{DS} voltage, if necessary). When the V_{GS} is below the threshold voltage V_{th} ($V_{GS} < V_{th}$), the structure remains the same as in equilibrium, and no current can flow (the P-region blocks the movement of electrons from the drain to the source).

When V_{GS} exceeds the threshold voltage ($V_{GS} > V_{th}$), an N-type channel forms in the P-type semiconductor along the oxide layer, as depicted in the diagram. Electrons can then flow through this channel from the drain to the source, accelerated by the V_{DS} voltage. Increasing V_{GS} expands the channel's cross-sectional area, reducing its resistance and increasing the current flowing through the channel. The channel behaves like a simple resistor, with a linear relationship between the current I_{DS} and the voltage V_{DS}.

$$I_{DS} = K(V_{GS} - V_{th})V_{DS} \quad (1)$$

with K, a constant that depends on the materials and the geometric parameters of the transistor.

Note: The voltage applied to the MOS capacitor is not the same at the drain and the source. Specifically, at the source: $V_{MOS|Source} = V_{GS}$, and at the drain: $V_{MOS|Drain} = V_{GS} - V_{DS} < V_{MOS|Source}$. Therefore, the channel is wider at the source than at the drain. This is because, at the drain, the V_{MOS} voltage is lower and closer to the threshold voltage, making it closer to the point where the channel may disappear.

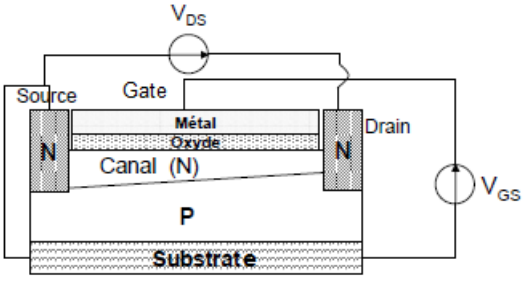


Figure 4: MOS Transistor in the linear regime.

In the pinch-off regime, increasing V_{DS} beyond a certain value (V_{DSsat}) causes the MOSFET channel to disappear at the drain side, while it remains formed at the source. This transition marks the end of the linear regime, as the drain-source junction no longer behaves like a simple resistor. Instead, a depletion region forms, limiting the current, which no longer increases with V_{DS}**.**

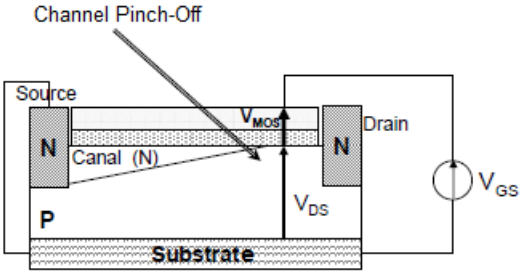


Figure 5: MOS Transistor in the pinch-off regime.

In the pinch-off regime, the following relation holds:

$$V_{GS} - V_{DSsat} = V_{th} \tag{2}$$

There are three main types of applications, which derive from the previous states:

- **Controlled switch**: The Gate-Source voltage controls the existence of the channel. This allows the drain-source circuit to be opened ($V_{GS} < V_{th}$) or closed ($V_{GS} > V_{th}$) using the Gate-Source voltage. This application is widely used in current digital electronics as well as power electronics.
- **Variable resistor**: The channel resistance can be controlled using the Gate-Source voltage (in analog electronics) by operating in the linear regime.
- **Current source and amplifier**: In the saturation regime, the MOSFET acts as a current source, where the current remains constant as V_{DS} increases.

The figure below shows the static characteristics of the different types of MOS transistors.

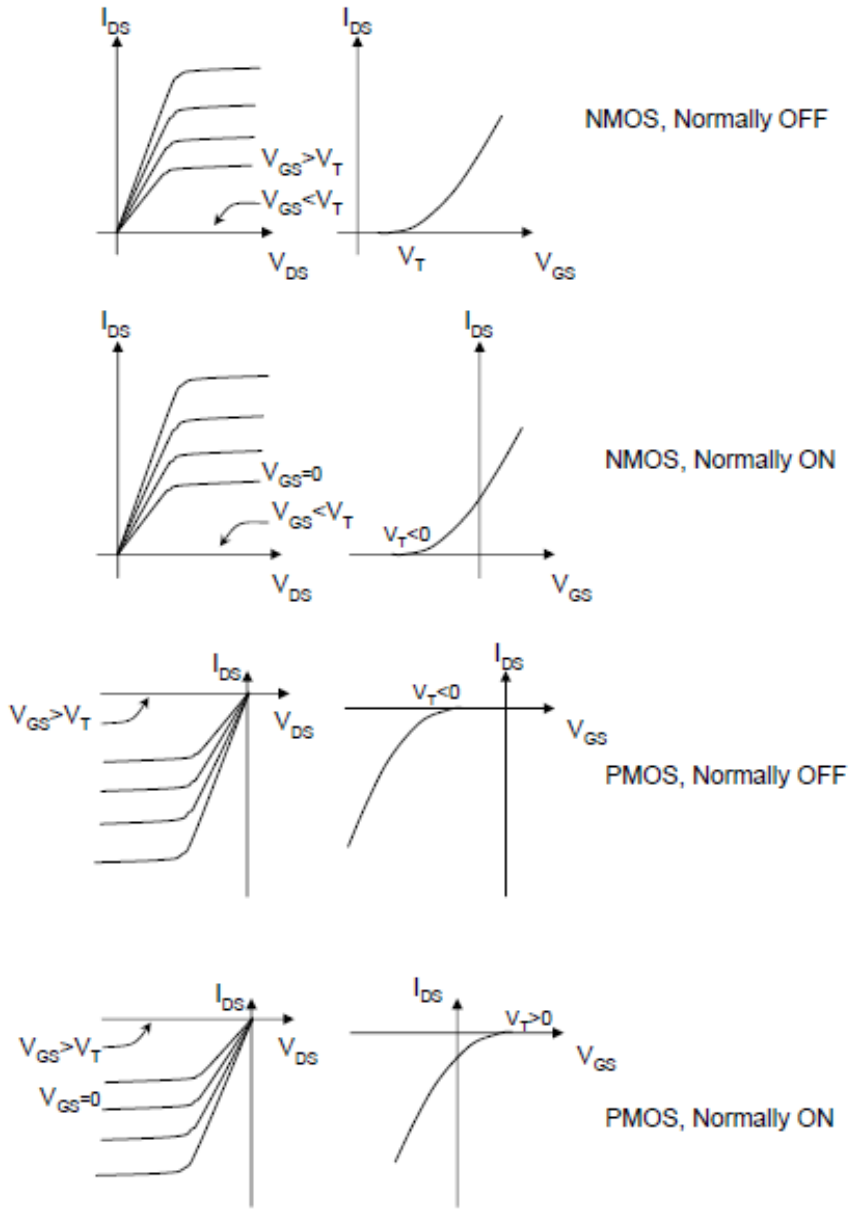


Figure 6: Static characteristics of the different types of MOS transistors.

Thus, we transition from a NORMALLY ON to a NORMALLY OFF by shifting the threshold voltage, and we switch from an NMOS to a PMOS by reversing the signs of the voltages and currents, meaning we take the curves that are symmetric with respect to the origin.

IV. Materials and Equipment

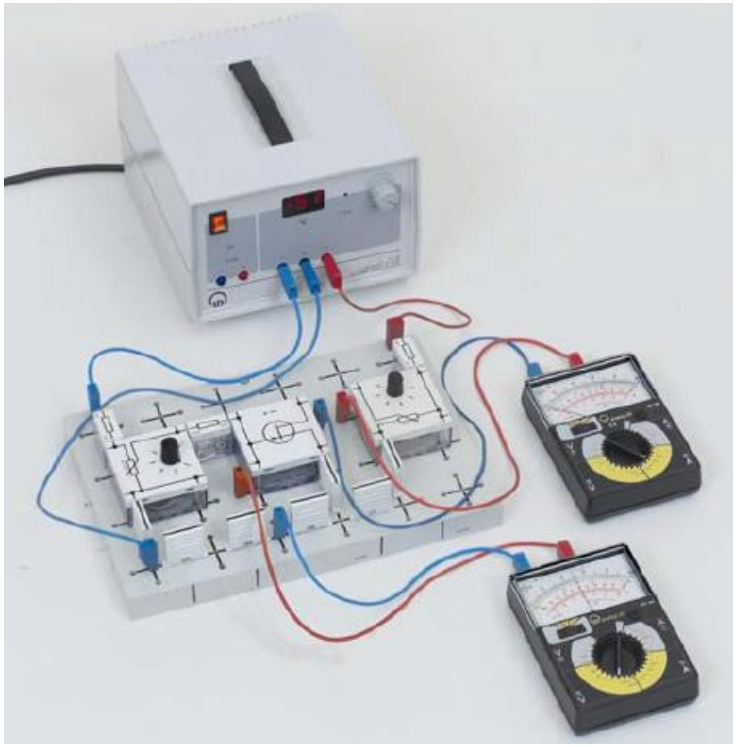


Figure 7: Experimental setup.

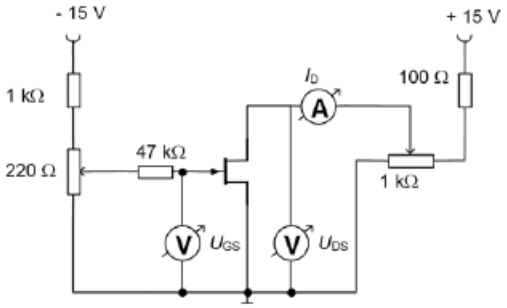


Figure 8: Basis circuit diagram for studying the characteristics of a MOS transistor.

V. Procedure

- Place the MOSFET on a breadboard. Identify the terminals: Gate (G), Source (S), Drain (D), and Substrate (B). Make sure to connect the Source terminal to ground.
- Connect a DC power supply to the Drain and Gate terminals, ensuring that they can provide a variable voltage range for both V_{DS} and V_{GS}.

- Set the V_{GS} to the desired value, and apply a small V_{DS} (typically 1V to 5V) to begin with. (This will help to observe the linear characteristics of the MOSFET in the initial stage).
- Gradually increase the V_{DS} voltage to observe the transition into saturation or pinch-off.
- Use a multimeter to measure the I_{DS} (drain current) for different values of V_{DS} while keeping V_{GS} constant. (This will give the I-V characteristic curve in the linear or saturation region).
- For a given V_{GS}, increase V_{DS} and record the I_{DS} values. Repeat this process for different V_{GS} values (e.g., $V_{GS} > V_{th}$ and $V_{GS} < V_{th}$) to study the behavior in various regimes (cut-off, linear, and saturation).
- Gradually reduce V_{GS} to find the threshold voltage (V_{th}), which is the minimum voltage required at the gate to form a conductive channel. This is the point at which the MOSFET begins to conduct significantly.
- Check the I_{DS} value for V_{GS} below and above V_{th} to confirm the transition between the cut-off and linear regions.
- In the linear region, where V_{DS} is small, $V_{DS} < (V_{GS} - Vth)$, the current should increase linearly with V_{DS}. Observe and confirm this behavior by increasing V_{DS} while keeping V_{GS} constant.
- As V_{DS} exceeds the threshold for saturation ($V_{DS} > V_{GS} - V_{th}$), the current should saturate and become independent of V_{DS}. This is the region where the MOSFET behaves like a current source.
- For high V_{DS}, at the pinch-off point (V_{DSsat}), the channel near the drain becomes constricted, and the current is limited by the P-region near the drain. Observe this characteristic when V_{DS} is increased further.
- Based on the collected data, plot the I-V curves for the MOSFET and analyze the operating regions (cut-off, linear, saturation). Compare the results with theoretical models.
- From the I-V characteristics, determine the threshold voltage (V_{th}), the transconductance (gm), the on-resistance ($R_{ds}(on)$), and drain current for various V_{GS} and V_{DS} values.
- Summarize your findings regarding the MOSFET's operation in different regions and its key parameters.
- Discuss any discrepancies with theoretical predictions.

Lab 5

Applications of PN Junction diodes

Lab 5: Applications of PN Junction diodes

I. Principle

The principle of the lab on junction diode applications is centered on the experimental analysis of their behavior in various electrical circuits, aiming to understand their functions and practical applications.

II. Objectives

- Understand the application of junction diodes in different electrical circuits.
- Rectify alternating voltage using junction diodes in both single and double half-wave.
- Smooth voltage with a capacitor (filtering) in rectifier circuits.

III. Theoretical Reminder

In Lab 2, we covered a theoretical overview of the operating principles of junction diodes. We analyzed their characteristic curves (I_d, U_d) in both forward and reverse bias and identified their main parameters. In this Lab, we will focus on the different applications of these diodes in electronics.

Electronic devices operate on direct current. To convert an alternating signal into a continuous one, the junction diode is primarily used. The most common diode applications include single-phase and dual-phase rectification.

Rectification is the process of converting an alternating voltage into a unidirectional voltage, known as the rectified voltage. This conversion is achieved using junction diodes.

There are two types of rectification:

- **Single-Phase Rectification**: When an alternating voltage is applied to the anode of a diode, only the positive half-waves will appear on the cathode (K). If the voltage is applied to the cathode, only the negative half-waves will appear on the anode (A). The output voltage will be reduced by approximately 0.6V, which is the threshold voltage where the diode starts to conduct. This means the potential difference across the diode is 0.6V, resulting in:

$$U_e > 0, \quad U_s = U_e . \frac{R}{R_d + R} \tag{1}$$

$$U_e < 0, \quad R_d \approx \infty, \quad U_s = 0 \tag{2}$$

$$U_s = U_e - U_d \tag{3}$$

$$U_{s,moy} = \frac{U_{s,max}}{\pi}, \quad U_{s,eff} = \frac{U_{s,max}}{\sqrt{2}} \tag{4}$$

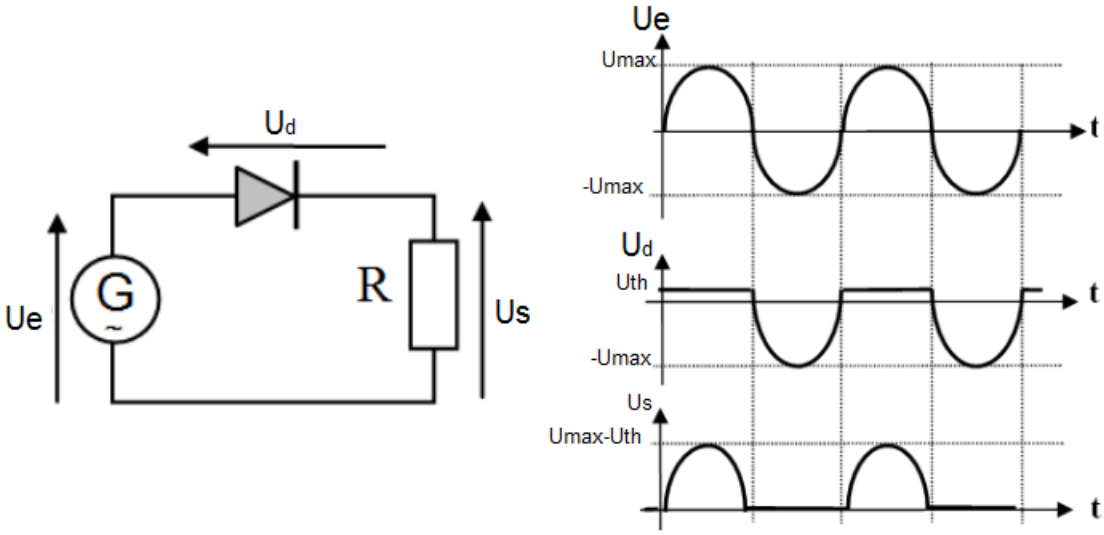


Figure 1: Single-Phase rectifier circuit.

- **Full-Wave Rectification**

During the positive half-cycle (+): Diodes D2 and D4 conduct, while diodes D1 and D3 are reverse biased and do not conduct. During the negative half-cycle (-): Diodes D1 and D3 conduct, while diodes D2 and D4 are reverse biased and do not conduct. The output voltage decreases by 2 times 0.6V, which is the threshold voltage at which both diodes start to conduct. This means the potential difference across each diode is 0.6V, resulting in:

$$U_e > 0, \quad U_s = U_e . \frac{R}{2.R_d + R} \tag{5}$$

$$U_e < 0, \quad R_d \approx \infty, \quad U_s = 0 \tag{6}$$

$$U_s = U_e - 2.U_d \tag{7}$$

$$U_{s,moy} = \frac{2.U_{s,max}}{\pi}, \quad U_{s,eff} = \frac{U_{s,max}}{\sqrt{2}} \tag{8}$$

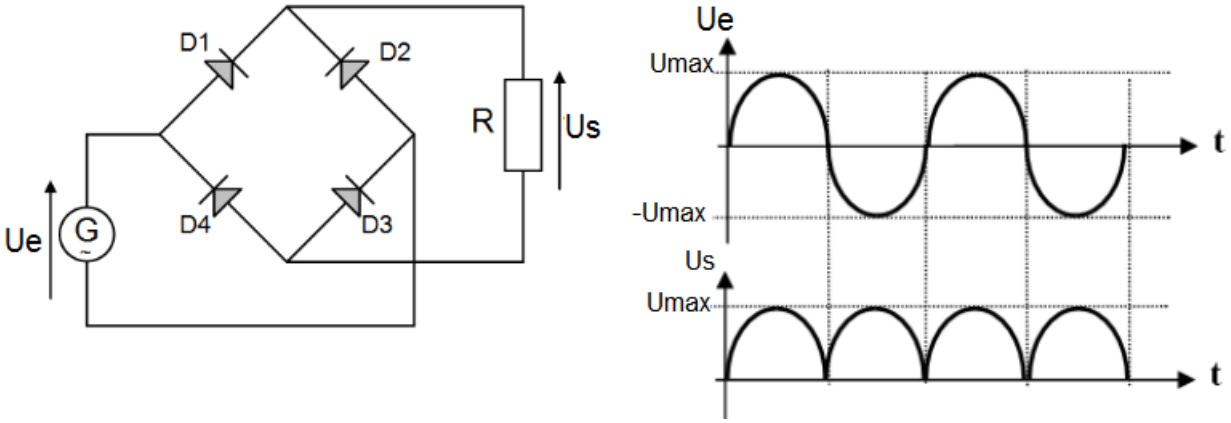


Figure 2: Full-Wave rectifier circuit.

- **Filtering:**

Filtering converts a rectified voltage into a voltage that remains as steady as possible. The most straightforward filtering component is a capacitor placed across the load (in parallel with the load). The capacitor functions as an electrical charge reservoir. The main characteristic of a capacitor, much like a reservoir, is its capacitance, C. The capacitor charges each time the pulsating voltage exceeds the voltage across the capacitor. The charging time constant depends on the diode's forward resistance ($Tc = R_d \times C$).

The charging and discharging rates of a capacitor are determined by the R_C time constant. In rectifier circuits with a resistive load (R) and a capacitive filter (C), the product RC defines the circuit's time constant $T_d=R\times C$, where T_d is the discharge time constant, measured in seconds.

The capacitor discharges whenever the pulsating voltage drops below the voltage across its terminals. It then discharges gradually through the load resistance R following the discharge time constant T_d. The effectiveness of the filter relies on this relationship.

The capacitance value affects the nature of the output voltage. The larger the capacitor value C, the closer the output voltage will be to a stable DC voltage.

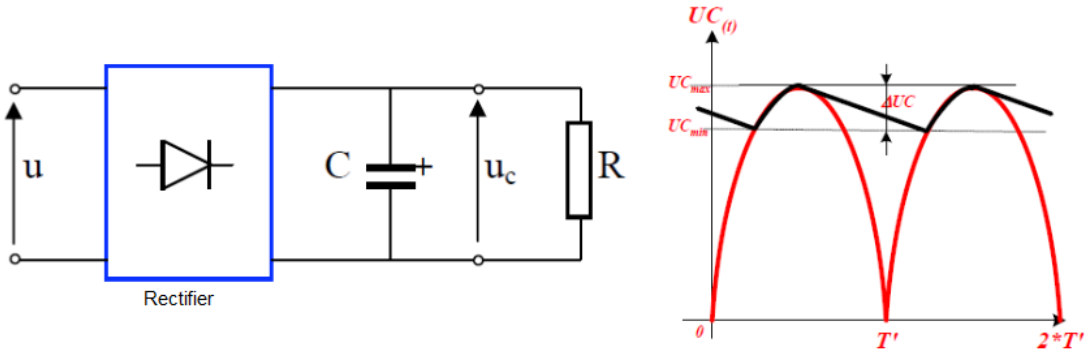


Figure 3: Circuit for filtering a rectified voltage.

After filtering, the voltage across the capacitor varies between a maximum value U_{Cmax} and a minimum value U_{Cmin}. U_{Cmax} = Maximum output voltage of the rectifier. U_{Cmin} = Minimum voltage required for operation (Stabilization or regulation). Its average value can be considered equal to:

$$U_{Cmoy} = \frac{U_{Cmax} + U_{Cmin}}{2} \tag{9}$$

The ripple around this average value is:

$$\Delta U_C = U_{Cmax} + U_{Cmin} \tag{10}$$

IV. Materials and Equipment

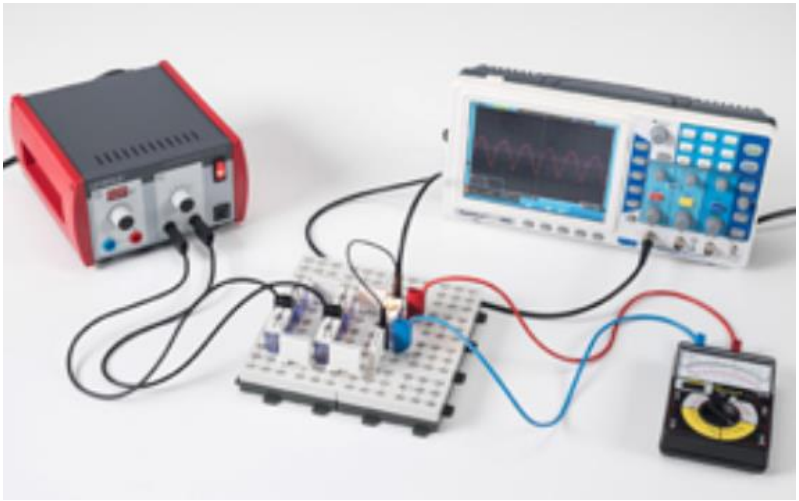


Figure 4: Experimental setup.

V. Procedure

a) Experiment 1

- Set up the circuit as shown in Figure 3, using a 2V amplitude source and a 1kHz frequency.
- Position one voltage probe before the diode and another after diode D1 (1N4009). Observe both signals with the following settings: START time: 4 ms, END time: 6 ms, TMAX: 1e-007 sec
- Plot the curves on a graph and white your observations.

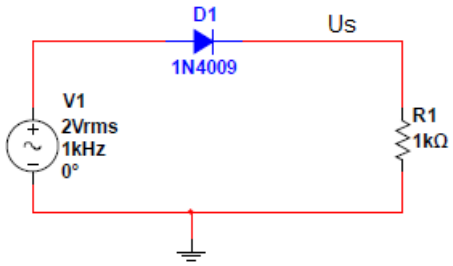


Figure 5: Single-Phase rectifier circuit.

b) Experiment 2

- Replace D_1 with a 1N1199C diode.
- Observe Us and Ue, then record your observations.

- **Experiment 3**

- Place a 1µF capacitor in parallel with resistor R_1, using the 1N1199C diode.
- Visualize the output voltage and plot the curve on the previous graph.
- Increase the capacitor value to 10µF, and then record your observations.

c) Experiment 4

- Construct the circuit shown in Figure 4.
- Observe the input and output voltages using a diode bridge (1B4B42), with the following settings: START time: 4 ms, END time: 6 ms, Step time: 10^{-7} sec
- Plot the curves on the graph. Us=Ue, then record your observations.
- Replace the bridge with a 3N250, and observe the input and output voltages.

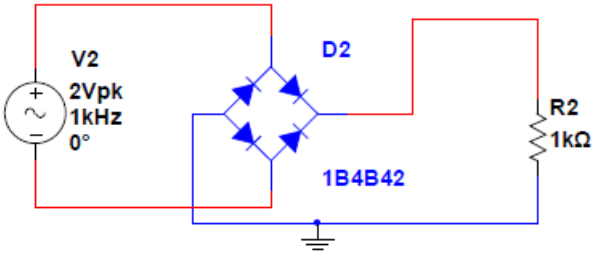


Figure 6: Full-Wave rectifier circuit.

- Place a 1µF capacitor in parallel with resistor R_1, using the 1B4B42 diode bridge.
- Visualize the output voltage and plot the curve on the same graph as before.
- Increase the capacitor value to 10µF, and then record your observations.

References

1. Neamen Donald A., "Semiconductor Physics and Devices: Basic Principles**",** McGraw-Hill Education, 2021 (4th Edition).
2. Simon M. Sze, "Physics of Semiconductor Devices", John Wiley & Sons, 2021 (4th Edition).